Summary SSIE 2024

The Summer School of Information Engineering (SSIE) 2024 was held in Brixen from July 8th to July 12th. The School is divided in two track, the first one on Machine Learning and its Applications, and the second on GaN and related materials. The Track 2 counted in total 37 participants and 13 invited speakers. The topics of the school were carefully selected to cover all the different aspects of the GaN technology, from crystal growth and device processing to reliability, with insights on the industrial and final applications.

To favor the interaction and networking between the attendees, several social activities were organized, including the "Brixen Mountain Carts" and a dinner.

The participants also had the chance to present their research work during the Student Workshop, an afternoon session with 12 presentations by students. The best presentation and runner-up were awarded a joint award from the Department of Information Engineering of the University of Padova and IEEE Italy section.

The SSIE guarantees also 5 ECTS after completion of a final test with multiple choice questions on the talks. 23/24 participants of the test got a sufficient evaluation and were awarded with the credits.

The program of the School is reported in the table below.

Monday July 8, 2024		
9:00	**WELCOME ADDRESS and LOGISTICS – Gaudenzio Meneghesso (University of Padova)**	
9:30	Maria Eloisa Castagna	**STMicroelectronics**, GaN-on Si power and RF: devices and application
11:00	**Break**	
11:30	Christian Koller	**Infineon**, The effect of charge trapping in GaN-on-Si HEMTs and strategies to mitigate them
13:00	**Lunch**	
14:30	Piet Vanmeerbeek	**BelGaN**, Power GaN technology from a physics point of view: why and how?
END OF DAY 1, 16:00		
Tuesday July 9, 2024		
9:00	Michal Bockowski	**UNIPRESS**, Insights on GaN bulk growth and ultra high pressure annealing
10:30	**Break**	
11:00	Hahn Herwig	**AIXTRON**, Mastering and innovating GaN epitaxy on Si
12:30	**Lunch**	
14:00	Fabrizio Roccaforte	**CNR**, Contacts and dielectrics in GaN devices: physics and technology
END OF DAY 2, 15:30		
Wednesday July 10, 2024		
9:00	Christian Huber	**Bosch**, Vertical GaN on foreign substrates: Concepts, challenges and perspectives
10:30	**Break**	
11:00	Farid Medjdoub	**CNRS**, Recent results on vertical GaN on foreign substrates
12:30	**Lunch**	

14:00	Tommaso Caldognetto	**University of Padova**, Applications of Wide Bandgap Transistors in Power Conversion Circuits
END OF DAY 3, 15:00		
Thursday July 11, 2024		
9:00	Matteo Buffolo	**University of Padova**, Future perspectives for GaN and SiC power transistors & the role of defects in the reliability of wide-bandgap devices
10:30	**Break**	
11:00	Schulz Juergen & Tayyab Muhammad-Farhan	**VALEO**, Trends for future automotive power electronics
12:30	**Lunch**	
14:00	**STUDENT WORKSHOP – Presentations from PhD Students**	
END OF DAY 4, 17:00		
Friday July 12, 2024		
9:00	Manuel Fregolent	**University of Padova**, Vertical GaN: reliability and trapping
10:30	**Break**	
11:00	Giovanni Verzellesi	**UNIMORE**, TCAD modeling of GaN-based RF and power devices
12:30	**BEST STUDENT PRESENTATION AWARD CEREMONY – Gaudenzio Meneghesso (University of Padova)**	
13:30	**5 ECTS FINAL TEST**	
END OF DAY 5, 14:00		

Summary of the Talks

In the following section, a summary of the talks is presented.

Maria Eloisa Castagna – STMicroelectronics

GaN-on Si power and RF: devices and application

STMicroelectronics's talk was held by Maria Eloisa Castagna, that gave an introduction to ST Microelectronics. After a presentation on the properties and composition of GaN from the physics point of view, she presented a scheme on the approach taken by the company on the manufacturing of GaN devices. She emphasized the importance of simulations, characterizations and reliability needed for this technology. The importance of collaborations with academic realities like the University of Padova to help the industry to have an insight on possible mechanisms that impact the reliability of GaN devices. With this she then introduced the main issues of GaN HEMT devices like current collapse, threshold voltage and the correlated physical effects that give such issues. She then introduced also some layouts and specific characterization techniques used to measure such characteristics. To end the presentation she also talked about GaN technology for RF applications, showing the greater performance of GaN over other semiconductors like silicon especially concentrating on the frequency capabilities. From this presentation was clear the workflow for GaN devices manufacturing and why GaN is preferrable over other technologies for power and RF applications with also some application case studies.

Christian Koller – Infineon

The effect of charge trapping in GaN-on-Si HEMTs and strategies to mitigate them

The message of this talk is that defects are an integral part of GaN devices that can't be avoided. Consequently, it is important to understand how they come into play and how they degrade the performance of the device in order to minimize their impact.

After an introduction to the advantages of GaN HEMTs in power applications, the device working conditions are discussed (off state, semi-on, and on state) with the consequent instabilities induced by trapping:

- Shift in the threshold voltage value, induced by charge trapped mainly under the gate region
- Current collapse, induced by charge trapped mainly under the access region.

The analysis then focuses on the role of the carbon at the buffer layer: high carbon concentrations (e19 /cm3) are intentionally introduced as deep acceptors to avoid unwanted vertical current in the device vertical structure, making the buffer insulating. The drawback is that deep trapping centers are introduced.

Accordingly, a specific structure was designed to study the back gating effect induced on a nGaN – C:GaN layer combination. Considering the activation energy of carbon and the capacitive response of the test structure at different biases, it is concluded that there is no interaction between carbon and the valence band. However, to explain the dynamics observed during measurements, it is concluded that carbon sites are mainly located along threading dislocations: these are present because of the lattice structural defects in GaN and the carbon accumulation in their vicinity is responsible for a parasitic leakage path. The charge shift between carbon sites in threading dislocations is defined as "charge redistribution".
The presence of carbon near dislocations was verified with EELS investigation.

Then, the analysis focuses on TLM structures at different negative back bias conditions. The TLM current lowering is monitored and many concurring mechanisms are identified:

- Charge redistribution within the C:GaN layer
- Hole leakage through GaN:uid through defect-assisted band-to-band tunnelling
- Hole leakage through SRL and substrate, preferably at carbon defect states (like in GaN:C)

It is now investigated if the TLM back gating is also occurring during the off state condition in pGaN gate HEMT, at the access region. In this case, the analysis of the VTH shift shows other two processes, due to the lateral field:

- Lateral hole transport: negative VTH shift is accelerated by VDS.
- Lateral hole movement & electron-hole recombination

In semi on state, instead, hot electrons can overcome the surface barrier and get trapped at the AlGaN/SiN interface and the high number of interface defects may exceed the 2DEG density. Consequently, the current collapse is relevant.

In on state, the lateral field is negligible and holes are injected from the gate. Holes recombine with trapped electrons and the device is refreshed to its original state. It is observed that buffer traps recover faster than surface traps.

Piet Vanmeerbeek – BelGaN

Power GaN technology from a physics point of view: why and how?

BelGaN is a new fab/company, but it was present as a foundry since a lot of years, with different names. Since they believe that networking is important, they propose and realize the creation of GaN valley, a system to bring together companies from all over Europe with focus on all different aspects of GaN.

Why do we need GaN: consider for example the US case, in which you have that 67 % of energy is lost, and only 33 % is properly used. This is because of the different conversion processes, energy distribution and so on. Why is this happening? Consider the widely used silicon and the novel GaN:

- Si: efficiency at 95.5 % at each conversion step from production, voltage grids, medium voltage grid, transformer hubs, to power adapter —> 83 % overall efficiency
- GaN: efficiency at 98.5 % at each conversion step from production, voltage grids, medium voltage grid, transformer hubs, to power adapter —> 94 % overall efficiency

GaN is not extremely better than Si (if you look at only one conversion step) but if you look at the different conversion steps that are needed, its advantages are extremely clear. You do not only gain in efficiency. If you do smaller devices, you also reduce the weight and the overall size of the circuits, and thus also the cost. You can obtain lower size devices because, due to the higher critical electric field of GaN, you can obtain the same on-resistance of Si by using a thinner drift region. But, of course, this works properly only on paper, because there are a lot of other factors that are playing a role in the calculation of the relation between on-resistance and breakdown voltage. For example, for GaN HEMTs, contact resistance is playing a role because we cannot use Au (gold) in a Si CMOS compatible fab.

In general, how GaN can do what it is doing? Mainly thanks to spontaneous and piezoelectric polarizations, coming from the different electronegativity of the atoms. It works only in the Wurtzite structure (and not Zincblende), because we have a non-symmetric structure.

Michal Bockowski – UNIPRESS

Insights on GaN bulk growth and ultra high pressure annealing

It is from world war that scientists are keen on growing crystals. At the beginning studies and works were just for curiosity, but later on this became a fundamental part of the semiconductor world: nowadays 60% of the crystals are grown for semiconductor companies.

One of the main problems to face when growing crystal is the demand for very high temperatures, needed for high quality substrates, this can be overcome with high pressure, which is quite easier to handle.

The comparison between all the growth technologies can be made on the basis of 3 key parameters, which are: the material morphology, the structural quality of the product and the growth rate.

Through the years many method were used for the crystal growth, here listed from the most used and secured to the most advanced but still under development:

- HPVE:
  - Performed at ambient pressure and 1300K, this technique allows a relatively high growth rate (100-200 µm/h) but suffers from a phenomenon known as parasitic nucleation.
- HNPS method
  - Temperature gradient method based on the reaction between Ga and N at high pressure (1GPa) and high temperature (1800K). It offers a very high crystal quality, but very long growth thime.
- Ammonothermal Method
  - Characterized by a growth rate of about 1-5 µm/h, it is performed double temperatures chambers, where dissolving and growth zones are divided by a buffle. Pressure is around 1000-6000atm.

It offers very high quality GaN crystals, as long as there are high quality GaN hillocks.

Usually hillocks are created growing GaN seeds with HVPE method.

Herwig Hahn – AIXTRON

Mastering and innovating GaN epitaxy on Si

Aixtron is a company that produces deposition equipment for the compound semiconductor industry with headquarters in Germany and presence in 8 different countries. The company was founded in 1983 and it has since been the technology leader in complex deposition systems. The speaker introduced the portfolio of the company that offers a variety of MOCVD machines suitable for GaN Power and RF, LASERS, SiC Power, MicroLEDs and speciality LEDs. After the Blue LED boom

the majority of their machines are used for power electronics. Being leader in the sector means that 3 in 4 of all MOCVD systems sold worldwide are from AIXTRON.

The speaker introduced the different deposition techniques focusing majorly on the Chemical Vapour Deposition (HT CVD for SiC and MOCVD for GaN). It is important to find ourself at a temperature level at which the growth regime of the material is solely determined by the supply of precursors.

AXITRON has two main types of MOCVD reactors: CSS reactors and mostly vertical (old tech mostly used in university) and Planetary Reactors. The latter is a direct evolution of the Horizontal tube reactor that grants higher average growth rate and growth on multiple substrates at the same time.

An overview of the GaN-on-Si topic was given focusing on the challenges that have been overcome in the past 10 years like the mitigation of the dislocation due to the mismatch between the lattice constant of these two materials or the difference in thermal expansion coefficients. The most recent design for a GaN transistor was explained and compared to the previous versions especially in terms of the C-Doped Buffer. AXITRON showed how it is possible to fine tune the carbon doping in the barrier avoiding carry-over into the 2DEG channer that would reduce the conductivity.

In the last section of the lesson a talk on innovation took place discussing the challenges of introducing new structures (vertical GaN) and material (AlScN instead of AlGaN due to lower lattice mismatch with GaN).

Fabrizio Roccaforte – CNR

Contacts and Dielectrics in GaN Devices: Physics and Technology

The objective of the talk was to highlight the importance of optimizing electrical contacts from a manufacturing point of view. They include interfaces between metals, oxides and semiconductors, that have to be optimized for the correct operation of a HEMT device.

The talk started with an overview of transport mechanisms (TE for a Schottky contact, TFE and FE for an ohmic contact) and their dependence on i.e. carrier concentration. Then, contact resistance for ohmic contacts has been analyzed with its dependence on doping, temperature, barrier height, and it has been pointed out that it is a dominant component for smaller and low-voltage devices. Such resistance can be reduced by reducing barrier height and this can be accomplished by properly choosing the contact metal and by using multilayers with gold on top to reduce oxidation. The effect of the atmosphere during contact formation has been shown describing the effect of a oxidising atmosphere for a contact on p-GaN. As a conclusion of this general part, the impact of material properties, (e.g. dislocations) on local electrical properties, including barrier height uniformity, has been addressed.

The talk then addressed some particular case studies for contact formation:

- Ohmic contacts to AlGaN/GaN Heterostructures: updates needed to standard TFE model, using heterostructure properties to predict contact properties;

- Recessed ohmic contacts: total resistance decreased, transport changes from TFE to FE for thin films;

- GaN-on-Si with 200/300mm substrates: gold needs to be eliminated for CMOS process compatibility: use of low-workfunction metals and improvement of Ti/Al/Ti ohmic contacts with a carbon interfacial layer;

- Schottky contacts on AlGaN/GaN heterostructures: transport changes from TFE to TE depending on the applied voltage;

- Normally-off GaN HEMTs;

- Dielectrics: Al_2O_3 is the most common system, interface with GaN needs to be controlled, annealing can be performed;

As a conclusion, the take-home messages of this talk were:

- Interfaces are key building blocks for contacts;

- Device physics understanding helps in contact optimization;

- Novel interface engineering techniques are important.

Christian Huber

Vertical GaN on foreign substrates: Concepts, challenges and perspectives

The speech held by Christian Huber highlights the business prospective behind the Vertical GaN (vGaN) technologies: the high demanding electrification of automotive market is pushing the agenda towards wide band gap solutions, with faster switching, lower switching and conduction losses. Inside this evolving market, Vertical Gan is the most appealing solution for the traction inverters: with requirement such as miniaturization, high breakdown voltages and conduction through body-diode, lateral GaN HEMT cannot withstand the Vertical GaN solutions.

When talking about Vartical GaN transistor, there are a plethora of channel architectures, which have been demonstrated in literature with their respective pro’s and con’s, but, when it comes to the final application, a crucial aspects is the cost effectiveness of the adopted solution.

BOSH and its partners aim to answer a market demand with the YESvGaN project: what is a cost effective solution, able to meet the inverter’s requirements?

The solution is the YESvGaN membrane transistor, which merge the lateral GaN advantages with the Vertical SiC ones, obtaining low on-resistance at high blocking voltage, high on-currents and low substrate cost. Key elements of Christian’s talk were the substrate choose and the process of the device: cost effective substrate, and the backside process, with the deep reactive ion etching allowin to remove the silicon substrate, obtaining a fully vertical device with a backside drain.

Despite the cost-effective solutions, and the success of the YESvGaN project, there are still open challenges as the Mg implantation for area-selective p-type doping.

Farid – CNR IMM

Recent results on vertical GaN on foreign substrates

Baliga FoM well describes the motivations unders all the studies that involves GaN and SiC in nowadays: even the best Si transistor, based on super Junction is not able to achieve the operational performances of GaN devices.

High frequency operation, together with a higher BD electric field are the main advantages of GaN devices with respect to Si devices. Despite this, the material is quite new and some limitations are still affecting devices; in the following a list of the main problems and their best solutions.

- Device costs.
    - This mainly depends on the substrate on which GaN devices are grown. GaN on Si is one of the best compromises between costs and device performances.
- Dynamic R_{ON} increases.
    - Back barrier is responsible for trapping processes in the channel: a well optimized carbon doping process is helpful in this way. As an improvement, AlGaN back barrier can further mitigate the trapping phenomena.
    - Improvement in back barrier and nucleation layer can even prevent from vertical conductions.
- Normally off devices operation.
    - Many solutions were presented, such as recessed gate or the cascode configuration. At this moment the best choice Is to put a p-GaN layer under gate metal, that can lift the band diagram and reach normally off operation.

Another improvement that can make GaN devices more feasible for high voltage applications is the avalanche operation, which is not reachable with lateral devices.
Another limitation of lateral devices is related to HV operation, since to reach hived VBD, larger devices are needed.
The main solution to these two aspects is the development of vertical devices. These allow to vertically apply VDS, instead of laterally, allowing for smaller area devices.

The main challenges related to vertical devices are related to the level of defects that are present in the GaN buffer, where the actual channel is. This aspect depends on the substrate on which GaN buffer is grown (GaN on Si would lower the cost, but increase defects).ù
Other difficulties involve the need to have a back contact, that means that silicon substrate have to be removed to have access to GaN.
Last development show that vertical transistors are something that can be achieved even with low costs (GaN on Si), allowing for higher BD voltages and avalanche operation.

Tommaso Caldognetto - UNIPD

Applications of Wide Bandgap Transistors in Power Conversion Circuits

The rapid growth in microprocessor power demand, driven by advancements in artificial intelligence (AI) and machine learning (ML), has significantly increased the requirements for efficient power conversion circuits. Modern applications, particularly those requiring power up to 1000W, place a premium on both efficiency and thermal management. In this context, wide bandgap (WBG) semiconductors have emerged as a critical technology, offering substantial performance improvements over traditional silicon (Si) devices. Wide bandgap materials such as silicon carbide (SiC) and gallium nitride (GaN) are gaining traction in various market segments due to their superior electrical properties. SiC is predominantly used in automotive and mobility applications, where its high thermal conductivity and ability to operate at higher voltages and temperatures provide significant advantages. On the other hand, GaN is making inroads into the mobile and consumer electronics sectors, thanks to its high electron mobility and efficiency at high frequencies.

Wide bandgap transistors find diverse applications in power conversion circuits, ranging from battery charging and motor drives to converters for lighting and power electronics for LiDAR systems. In OFF-board charging stations, core functionalities include rectification, power factor correction (PFC), galvanic isolation, and output voltage regulation. Isolation transformers are particularly critical, as their volume is inversely proportional to the frequency, highlighting the need for high-frequency operation to minimize size. Enhancing a DC/DC stage requires incorporating isolation and output voltage regulation, typically targeting power levels in the tens of kilowatts. To achieve higher power outputs, multiple modules are often paralleled. However, achieving a wide output range and high efficiency remains a significant challenge. While LLC resonant converters meet many requirements, they fall short in modulating the switching frequency (F_{sw}) for output voltage regulation, as performance degrades when operating far from resonance.

To overcome the limitations of LLC converters, various strategies can be employed. These include rearranging the conversion circuit, utilizing resonant tanks, partial-power conversion, multiple stages, and optimizing both the primary and secondary sides through advanced control provisions. Zero voltage switching (ZVS) is crucial, particularly in half-bridge configurations, to prevent hard-switching events and reduce switching losses to zero. Several topologies are utilized to address these challenges:

- **LLC (basic)**: Provides the foundational resonant conversion but lacks advanced regulation capabilities.
- **BB-LLC (multistage + regulation stage)**: Incorporates multiple stages with an additional regulation stage for enhanced performance.

- **LLC+TBB (multistage + partial-power regulation stage)**: Offers superior performance with only a few additional components, combining multistage conversion with partial-power regulation for optimized efficiency and flexibility.

These advanced topologies enable wide bandgap transistors to achieve high efficiency and performance across a broad range of power conversion applications, meeting the demanding requirements of modern electrical systems.

LLC+TBB

The LLC+TBB topology is a sophisticated power conversion architecture that integrates an LLC converter operated as a DC transformer (DCX) with a twin-bus buck converter for voltage regulation between V2 and V1. This configuration leverages the strengths of both LLC and TBB stages to achieve high efficiency and performance across varying load conditions. The LLC converter operates at its resonance frequency (Fo) and switching frequency (Fs), maintaining operation in resonance. In a typical setup without DCX operation, the Fs/Fo ratio is adjusted to modify the voltage conversion ratio, which can lead to non-optimal performance due to dependence on the transferred power. However, when used as a DCX, the first harmonic equivalent circuit ensures a constant conversion ratio (unity) regardless of the power transferred. The circuit is composed of a half-bridge configuration on the primary side, followed by a resonating tank and a rectifier block on the secondary side. This configuration allows the primary side to achieve zero voltage switching (ZVS) and the secondary side to achieve zero current switching (ZCS). For the primary side, an 800V 20A setup uses a 1200V 30mOhm SiC MOSFET, while the secondary side (port rectifier) with 500V 30A employs a 650V 60A SiC PIN-Schottky diode. Additionally, the low voltage secondary side handles 230V 50A using a 400V 100A SiC high voltage rectifier. The twin-bus buck (TBB) stage addresses the maximum voltage stress between V1 and V2, resulting in lower switching losses by utilizing devices with lower voltage ratings, thereby achieving lower losses and higher efficiency. The TBB stage operates with a 300V 30A configuration using a 600V 30mOhm GaN FET with an integrated driver, providing isolated gate signals. An experimental prototype demonstrates the effectiveness of this topology with an 800V input and 250-500V output, delivering 10kW of power to a 90Ohm resistive load. The switching frequencies are Fs-LLC = 200kHz and f_{TBB} = 73kHz, achieving an efficiency of 98.4%. The switching frequency of the TBB can be modified to satisfy zero voltage switching (ZVS) if the load requires different power values, with the optimal f_{TBB} changing according to the delivered power (higher f_{TBB} with lower P_{del}). Online efficiency optimization is facilitated by Extremum-Seeking Control (ESC), a model-free adaptive control applied to an objective function with local extrema, ensuring optimal efficiency under any operating conditions. Without this optimization, transitioning from a 2kW to a 6kW load would result in losses amounting to 20% of the optimal value. Notably, the prototype achieves a record efficiency of 98.63% at 500V. The LLC+TBB topology exemplifies how advanced power conversion

architectures can achieve high efficiency, adaptability, and performance, making it a compelling choice for modern power electronics applications.

Interfacing the Electric Grid

The integration of bidirectional switches, made viable by GaN planar technology, offers significant advantages for interfacing with the electric grid. These switches operate ten times faster than equivalent discrete silicon solutions and provide cost savings by replacing four unidirectional switches with a single bidirectional switch. The bidirectional switches feature a shared drift region, are normally off, and have two gates with independent isolated driving, configured in a common drain setup. An example topology employing these bidirectional switches is the three-phase isolated buck matrix-type AC front-end. This design uses monolithic integrated bidirectional switches to achieve power factor correction (PFC) functionality without DC link capacitors. The primary side of the transformer operates with a six-segment PWM modulation, achieving zero voltage switching (ZVS) over a wide operating range, and utilizes space vector modulation. Simulation results comparing this converter with a benchmark circuit show that the losses in the benchmark circuit are higher in all cases. The proposed converter exhibits a flat efficiency curve, which is advantageous for various applications, with a maximum output current set to 25A.

Schulz Juergen & Tayyab Muhammad-Farhan – VALEO

Trends for future automotive Power electronics

The talk authored by Schulz Juergen and Tayyab Muhamm ad-Farhan from VALEO, tier 1 supplier of power devices for automotive applications, explores by a commercial and technological perspective the impact of inserting GaN in EV market sector. In this field, Si and SiC has doomed in the past years, the first thanks to its availability and low-cost, the second to its superior material properties and especially for the capability to reach high-frequency and reduce device's dimensions. However, more recenly also GaN E-mode and D-mode devices have become appetible for the market sector, not only for unique GaN properties that allows to compete with SiC in terms of high-frequency performance but especially for the possibility in reduction of switching loss thanks to a consistent decrease in reverse-recovery loss during operation. Key modules in which GaN should be inserted are the Inverter and the OBC DC-DC. In the first challenges remain open regarding the limited voltage range (650 V) respect to the 800V needed for the market as well as the relative large die area that yields to a necessary parallel layout implementation. For the second, increasing application frequency ranges enables reduction of magnetic components allowing to reduce form factor and increase efficiency, even if comparatively low amperage and costs still remain a problem. Despite the encouraging results, the need from a research point of view to ensure the reliability of GaN technology remains a must to finally introduce GaN in the market sector.

Manuel Fregolent – UNIPD

Vertical GaN: reliability and trapping

An extended overview of the role of wide and ultrawide bandgap semiconductors in power applications is provided, focusing on the advantages of innovative architectures as the vertical GaN MOSFET and Ga_2O_3 finFETs.

Vertical GaN devices have recently drawn attention as a promising alternative to overcome the limitations of lateral devices such as the absence of avalanche and the complicate field management. Moreover, other relevant advantages could be summarized as: reduced area consumption, better field management, higher operating voltage, avalanche capabilities, and MOS-like structure devices.

However, one of the most critical drawbacks is the important trapping processes ascribed by the foreign oxides at the gate terminal. Other trapping mechanisms are related to deep levels, dislocations, etc.

Considering the complexity of the structure, MOS capacitors (Al_2O_3 oxide) are investigated first with capacitive measurements (CV). Preliminary results show good stability of the structures between -2.5 V to 5 V, while higher positive gate voltage induces trapping with a rightwards shift of the CV, and more negative gate voltage induces a leftwards shift of the CV.

No thermal dependence was observed in the dynamics, suggesting that trapping centers are filled through tunnelling mechanisms, at the oxide border.

The negative bias stress was further investigated to understand an unusual hump in the dynamic with the support of the UV light, showing in both method coherence in the results: the conclusion is that negative bias activates interface states with activation energy around 0.6 eV.

This hypothesis was confirmed even with the support of simulations, where good agreement was achieved with real CV measurements, taking into account both interface and border traps.

Then, trapping in pseudo vertical GaN trench MOSFETs grown on Si-substrate is investigated. Firstly, a sequence of IDVG curves performed at increasing gate ramps shows a clear shift in the threshold voltage value that could be reset with the support of 365 nm UV light.

A gate stress analysis was then performed to investigate the shift in the threshold value, showing an important positive variation after 1000 s. This variation is only partially recovered during the following 1000 s at no stress condition, suggesting that traps are probably located at the oxide level. Moreover, this process seems to be independent by temperature and possibly related to tunnelling effects.

However, the recovery is enhanced if a negative voltage is applied instead of 0 V, due to the strong electric field at the gate region. A negative temperature dependence is observed, with a possible interplay with a gate leakage mechanism.

An increase in the threshold voltage value is observed even during the off state stress, with the device biased at a high drain voltage. Then, with the support of other measuring techniques, trapping sites located in the NPN stack are also identified.

Then, beta-Ga2O3 is discussed: this promising material has a higher breakdown field and good n-type doping. However, p-type doping has not been demonstrated yet.

Vertical β-Ga2O3 finFETs with different field plate configurations are now studied to investigate the threshold voltage value instabilities. An important shift is observed during gate stress.

Other insightful techniques to study these devices are based on optical analysis.

Giovanni Verzellesi – UNIMORE

TCAD modeling of GaN-based RF and power devices

The talk started initially with a description of the market share of Gallium Nitride devices. Moreover, a brief introduction to the main advantages of GaN Hemt for RF and power application was given. The first part of the talk considered a case of study of a planar RF device to explain the principle of trapping. The general aspect of trapping can be summarized as:

- The traps charge up and the trap discharge from the trapping sites are slower than changes of the bias.
- Traps can induce dynamical electrical effects like dynamic instabilities of V_{TH} and R_{ON}.
- Trapping is composed of two aspects: (i) “Traps location” (Surface, buffer, barrier...) (ii) “Trapping mechanism” (leakage, electric field...)
- A reduction of the drain current is associated with capture of electrons or emission of holes
- Traps in the access region affect mostly the transconductance (gm) and the R_{ON}.
- Traps in the gate stack, under the gate, are responsible for instabilities of the threshold voltage.

Subsequently the trapping in the buffer related to Iron and Carbon doping were explained in detail. Iron traps are usually activated when punch-through occurs (leakage current in the buffer). Carbon doping is usually adopted instead of Fe for the better control of the doping profile. However, Carbon is responsible for instabilities of R_{ON}, and long time constant. Different model of Carbon traps has been proposed, and the most recent one, involves the presence of two levels. A deep acceptor level at 0.9 eV from the valence band and the presence of a shallow donor level. Subsequently, a deep analysis of the physical mechanism responsible for the dynamic increase of the R_{ON} were analysed. More in detail, the trapping mechanism involves the emission of holes from the C_N acceptor traps, followed by a drift of the holes to the bottom of the traps where they get trapped again. The detrapping process is specular.

Moreover, different cases of study were presented and the concept of “virtual gate model” was introduced to explain the non-monotonic behaviour between CC, breakdown voltage increase and Carbon concentration in the buffer (at a certain C concentration CC reduce and the breakdown voltage stop to increase). Virtual Hole gate effects are related to surface traps which become active when electrons are trapped and become neutral when electrons are emitted. More in detail, during

negative gate stress (NGS) holes are emitted from the barrier traps and are removed from the gate. On the contrary, during positive gate stress (PGS) holes are injected and captured by barrier traps. P-GaN gate is responsible for the modulation of interface traps at the surface traps state.

Then different case studies were described to evidence the different degrading mechanism for devices with Iron or Carbon traps in the buffer. Step stress measurements in off-state has evidence a good stability for devices with Fe traps in the buffer, whilst devices with a C-doped buffer exhibited poor stability.

Considering the stresses in on-state, it was demonstrated that the presence of hot electrons may influence the trapping mechanism in the buffer. Even in this case devices with a Fe-doped buffer exhibited a good stability, in contras for what was observed for C-doped devices. The main reason is that Fe-related trapping is associated with electron trapping in the buffer, and fast time constants. C-related trapping is associated with the polarization of charge due to the emission of holes, and long time constant. During on-state stresses the electrons in the channel are collected by carbon traps (holes traps) leading to damage of the crystal lattice and may lead to semi-permanent degradation effect. By illuminating the devices with an UV light is possible to completely recover the device in a short time (if the light can reach the buffer), otherwise the recovery time constants are long.